Schematics for Dynapic and Dynasim Interfaces

Hereafter we present a few schematics which should serve as ideas for the design of interfaces for Dynapic and Dynasim keyboards.

Contents

1 DYSI-97 Interfaces

1.1 Introduction

In this chapter we present a few interfaces which were implemented using the ASIC DYSI-97.

- The ASIC DYSI-97 was produced especially as interface for Dynapic and Dynasim keyboards.
- The functionality of the DYSI-97 is based on the „oversampling“ technique, with which the electrical charge can be evaluated.
- Especially with „long-time“ the DYSI-97 is the best possible interface.
- The functionality of the DYSI-97 is described more detailed in the *Datasheet Dynapic and Dynasim Interface-Chip DYSI-97PS/PSK/S*.
- In applications with the DYSI-97PS the DYSI-97PSK can also be implemented.

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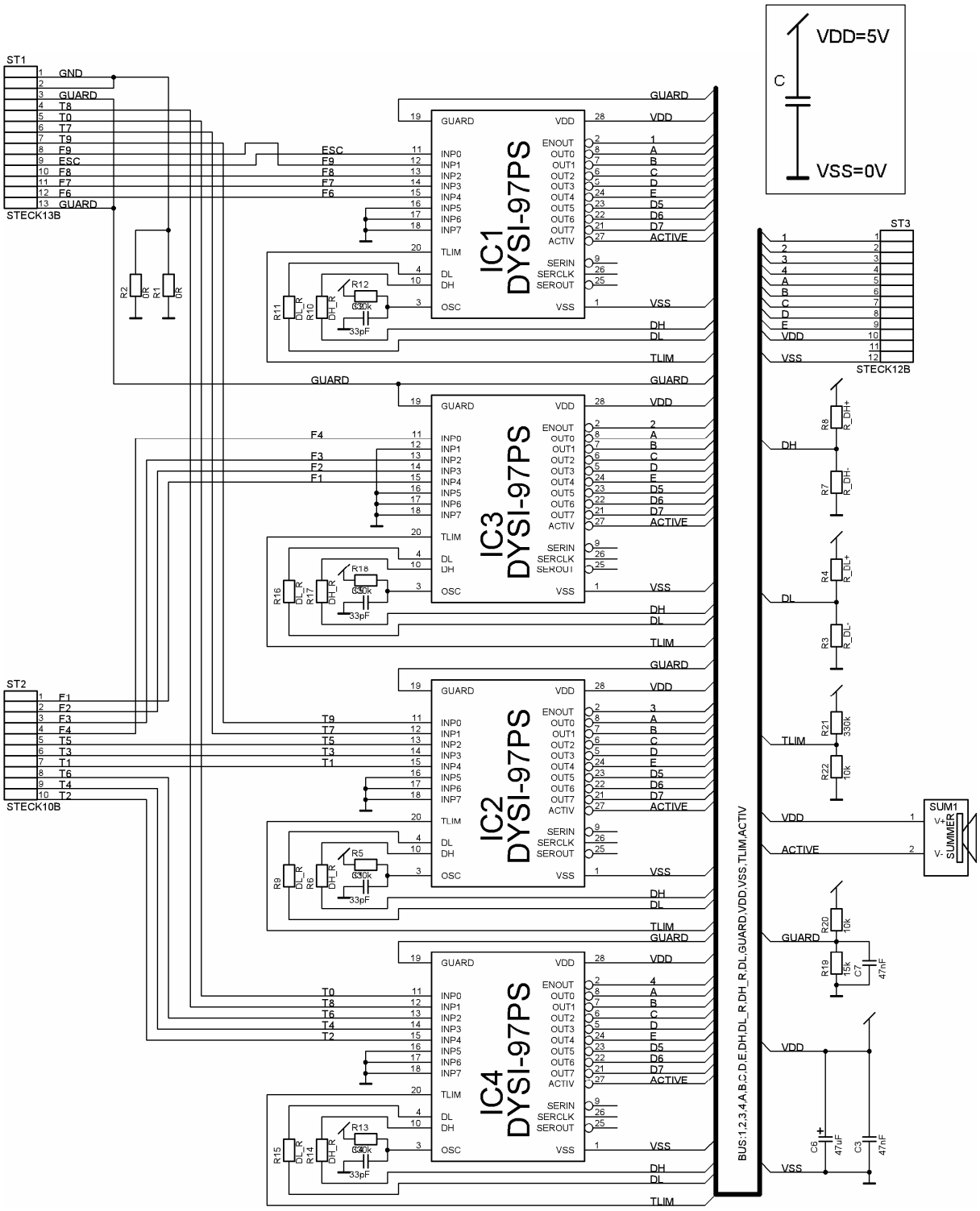
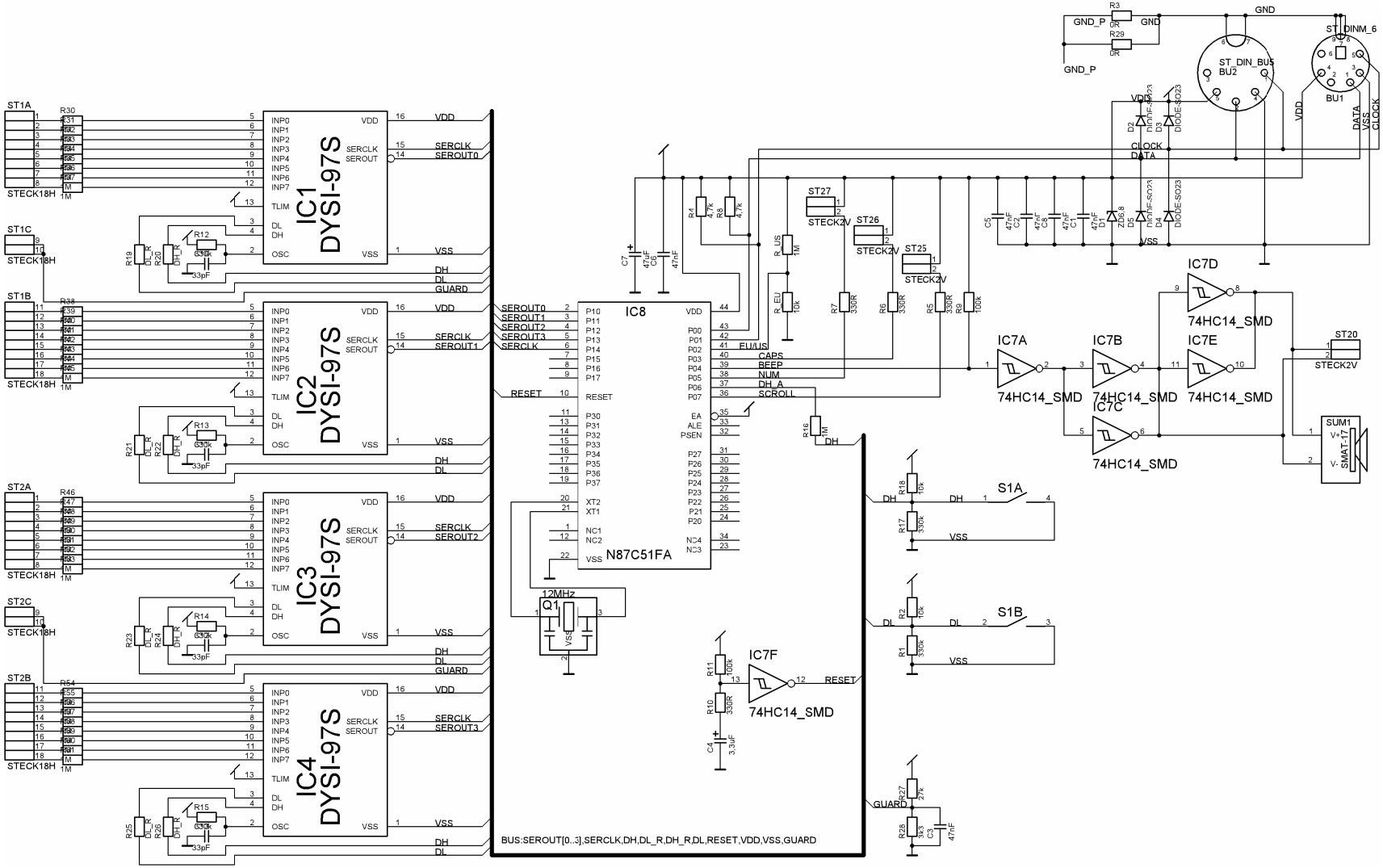
1.2 Matrix 4x8 for Dynapic and Dynasim

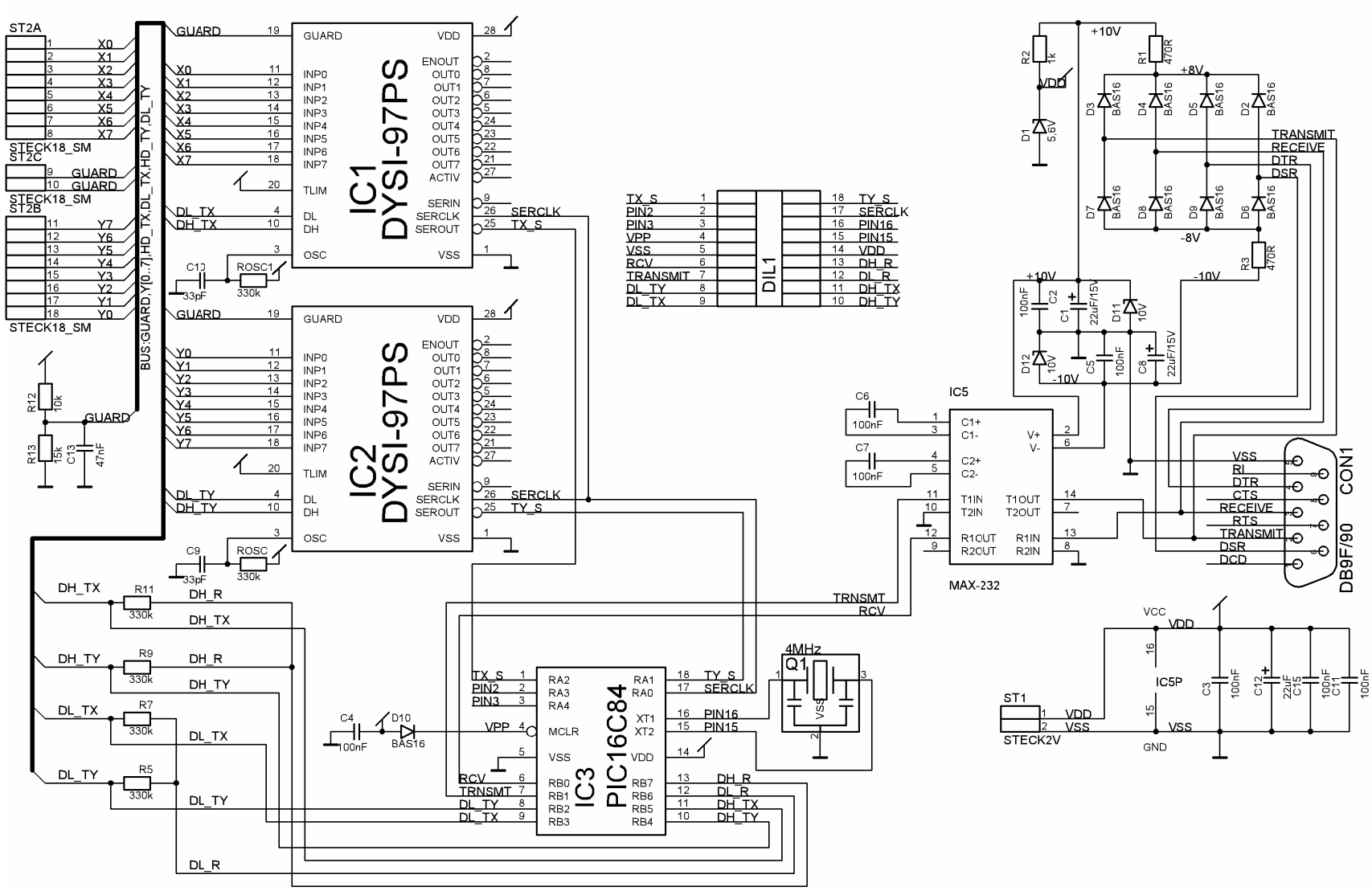
- The matrix is not fully formed, as for this application not all crosspoints in the matrix are used with keys.



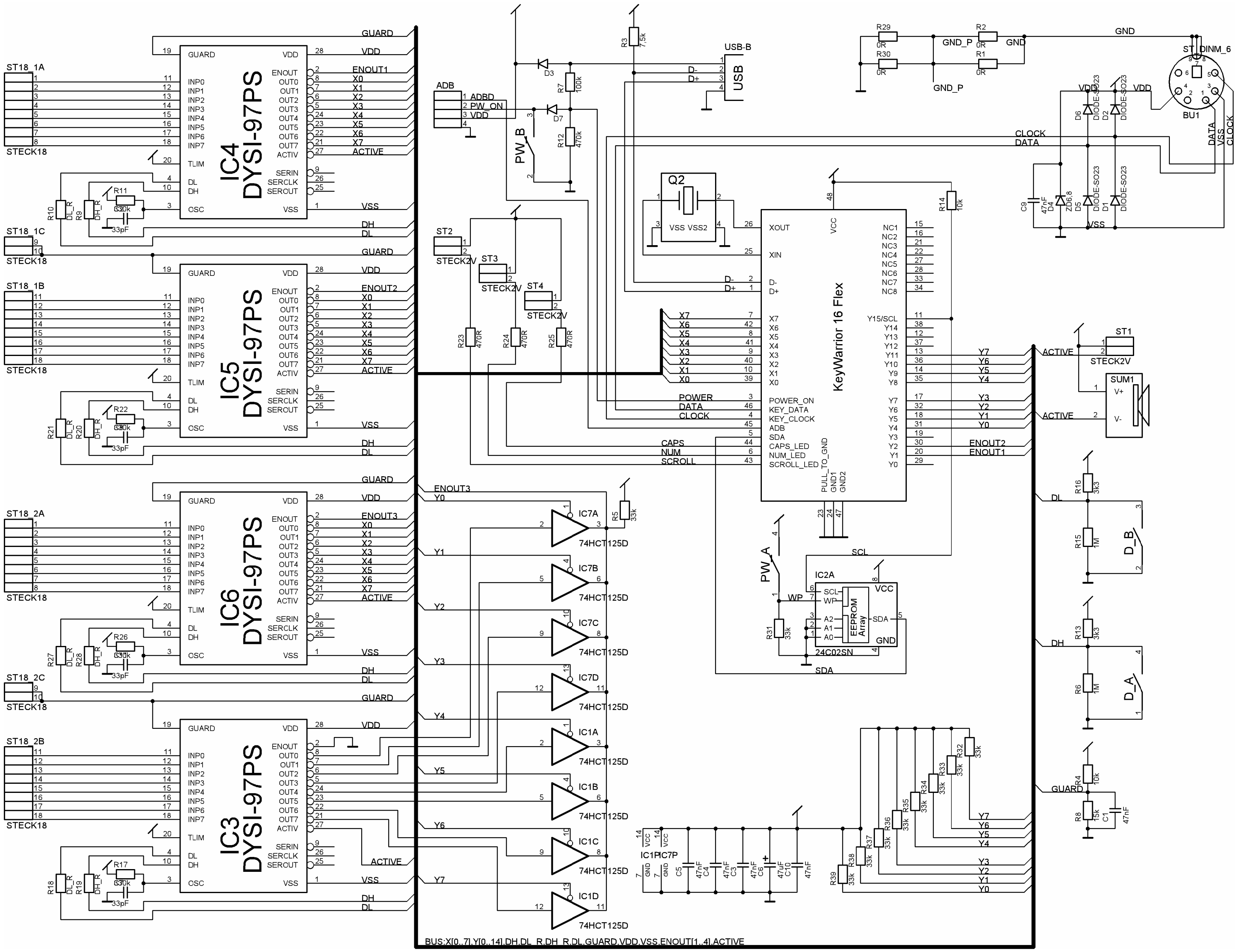
1.3 IBM-AT/PS2 for Dynapic and Dynasim



1.4 Serial Interface RS232 for Dynapic and Dynasim



1.5 Serial Interface USB and PS2 for Dynapic and Dynasim



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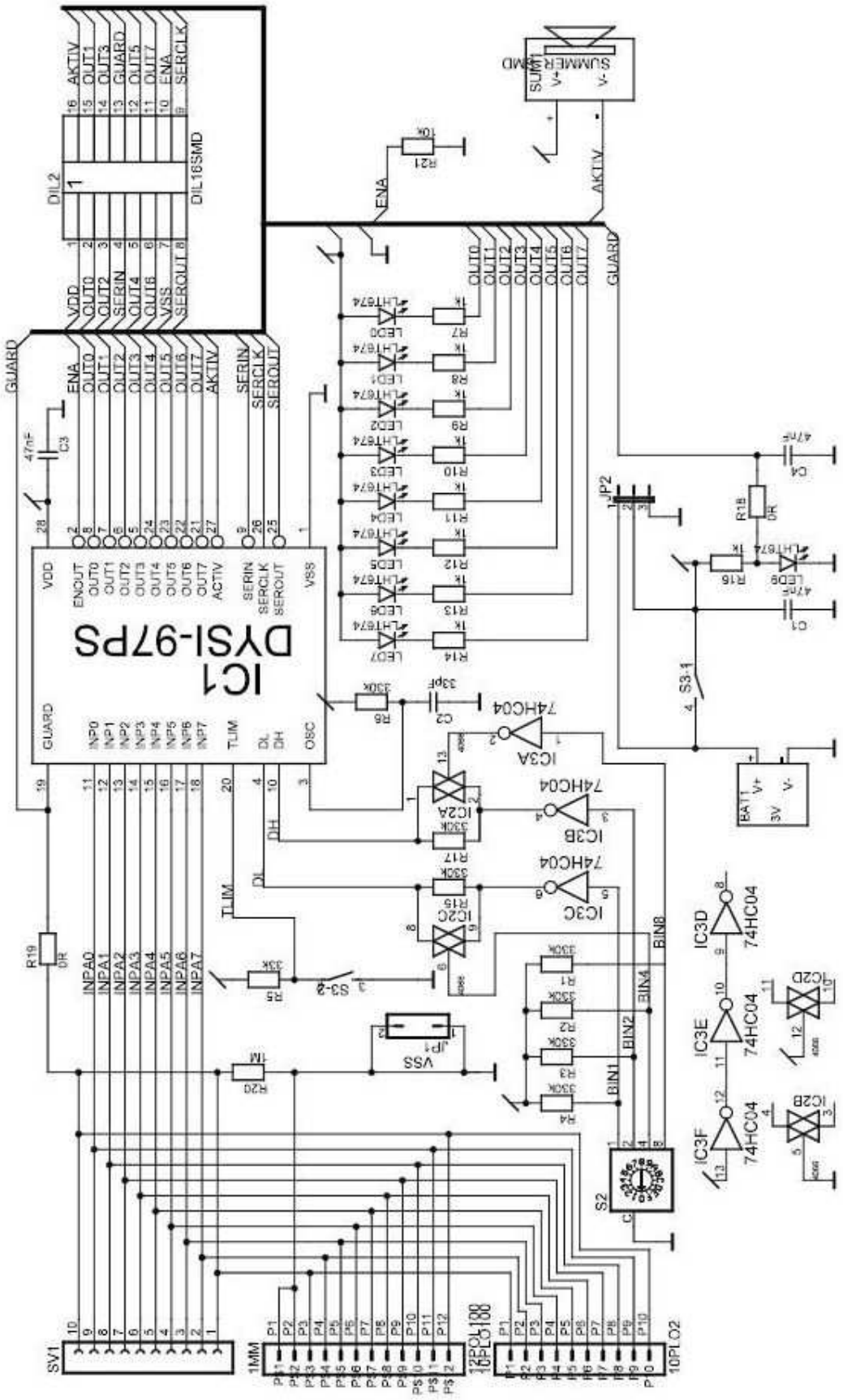
1.6 Interface OCT608 for tests for Dynapic and Dynasim



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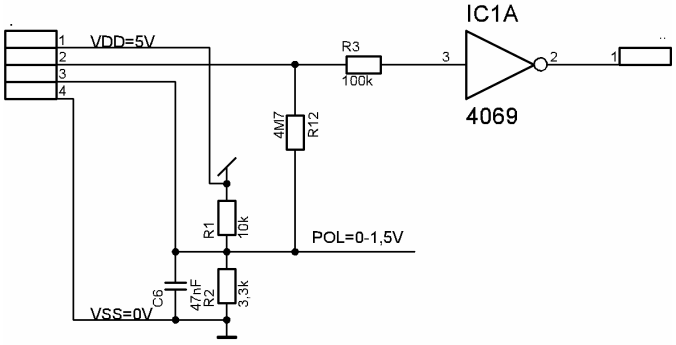
2 CMOS Interfaces

2.1 Introduction

- CMOS interfaces are good and cheap.
- Usually the CMOS interface serves to evaluate the voltage which the piezo element gives out when it is activated.
- The threshold can be adjusted within certain limits.
- The threshold is adjusted by increasing the common level of the piezo elements to a higher potential than 0V, e.g. to 1.2 V. Thus the piezo element has to give out only approx. 1.3 V to reach the threshold of the CMOS-IC of 2.5 V.
- Interfaces for long-term mode can be produced, but they are more costly.
- Voltage supply is necessary.
- For all the presented circuits a debouncing has to be planned if necessary. This can be realized either with a RC element or with a software programming.

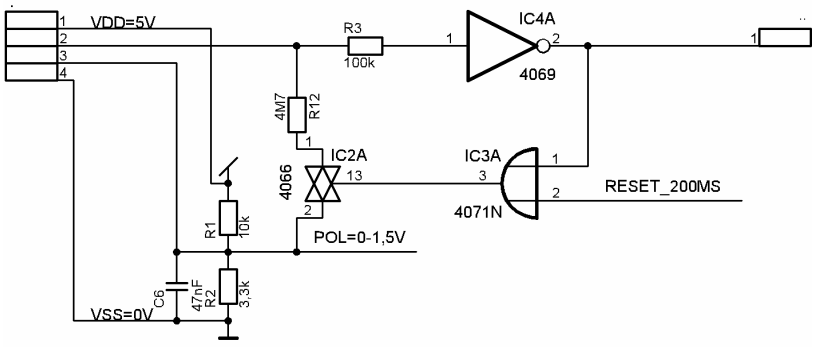
2.2 CMOS Interface with inverter

- The threshold (for all inputs together) is adjusted with the voltage POL.
- Instead of the inverter any other CMOS Gate out of the 4000 serial can be used.

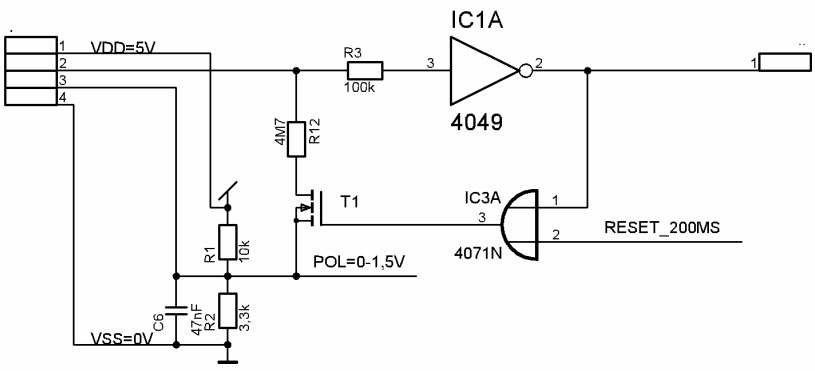


2.3 CMOS Interface with inverter and with long-time

- Enlargement of the circuit with inverter.
- The long-time is ensured with the analog gate.
- The long-time depends on how high ohmic the CMOS elements are.

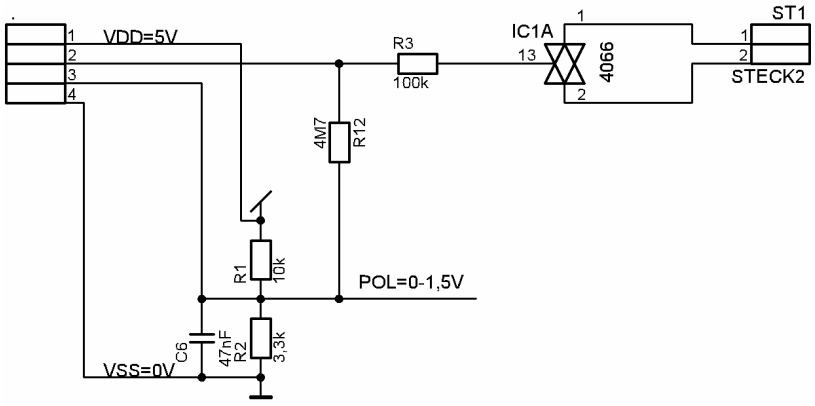


- Alternative, in case the voltage on the piezo (only Dynapic) is possibly higher than the voltage supply of the circuit.



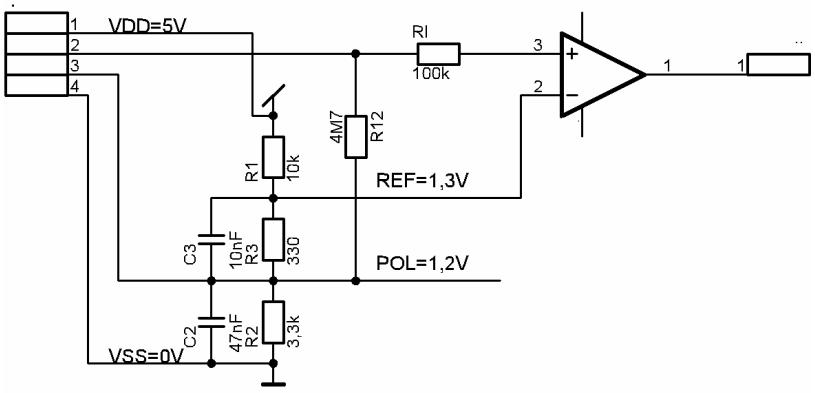
2.4 CMOS Interface as analog switch

- With this circuit a potential free switch (within the limits of the voltage supply) can be produced.



2.5 CMOS Interface with adjustable threshold

- In order to adjust the threshold very precisely in this circuit a CMOS comparator is used.
- An interface for large keys – with the according large capacity and small signal voltage – can be produced.
- The threshold in this example is approx. U_{th} = 0.1 V.

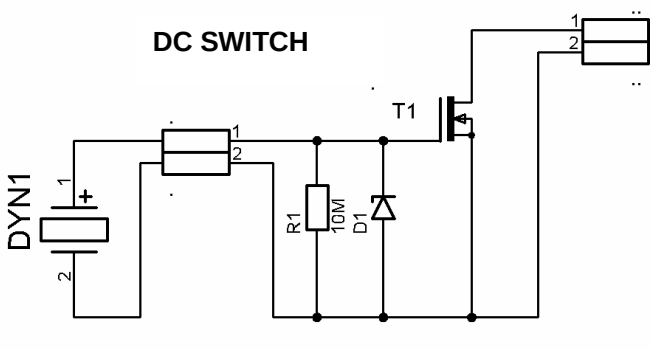


3 FET Interfaces

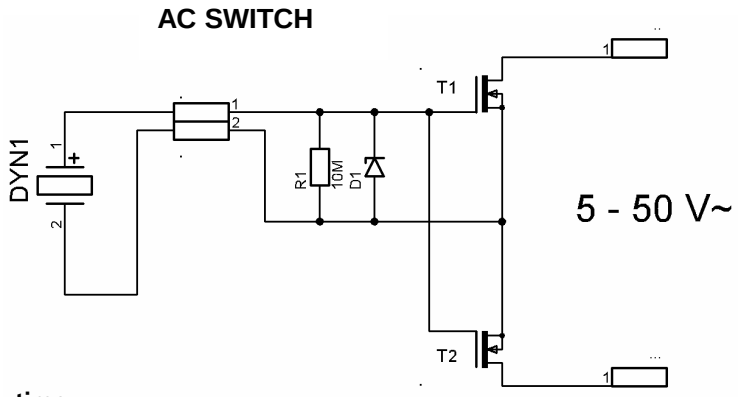
3.1 Introduction

- Interfaces with FETs can be applied where no voltage supply is available.
- In the case of an interface with FET the threshold mainly depends on the threshold of the FET and is therefore barely adjustable.
- For all the presented circuits with FETs bouncing can occur. This has to be taken into account when applied.
- Each FET must be protected with a Z-Diode at the input, if it is not already integrated.
- Since the Z-Diode has a leakage current depending on temperature, the long-time is depending on temperature, too.

3.2 FET Interface for DC

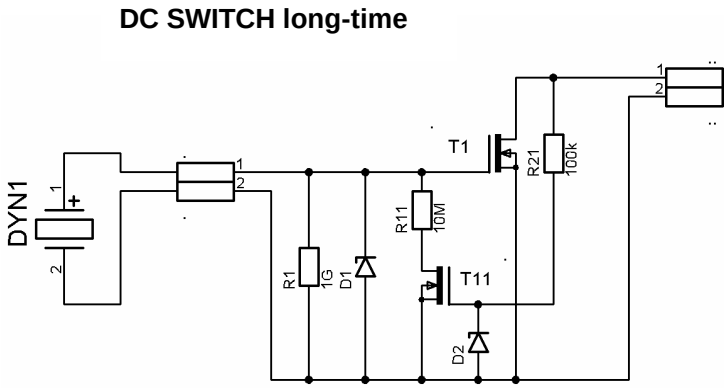


3.3 FET Interface for AC



3.4 FET Interface for DC with long-time

- The switching voltage is 5-50 V (the limit values depend on the FET types).
- Both FETs need a Z-Diode at the respective gate.
- The long-time is limited by the resistor R1, the leakage current of the Z-Diode, the leakage voltage of the FET and the capacity of the piezo element.



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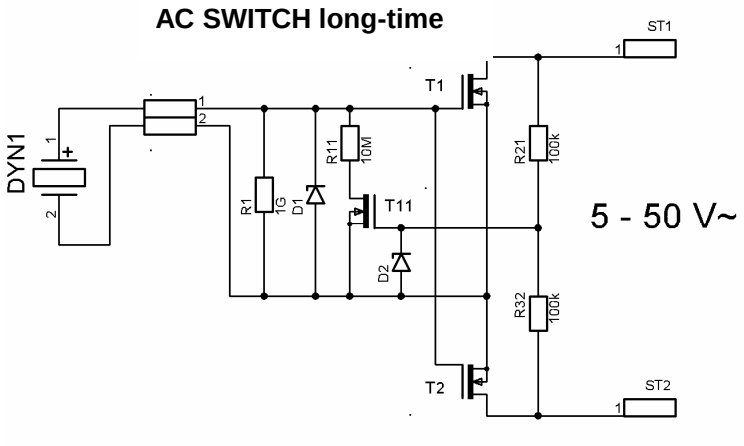
3.5 FET Interface for AC with long-time

- The switching voltage is 5-50 V (the limit values depend on the FET types).
- Both FETs need a Z-Diode at the respective gate.
- The long-time is limited by the resistor R1, the leakage current of the Z-Diode, the leakage voltage of the FET and the capacity of the piezo element.



4 Micro Processor Interfaces

4.1 Introduction

The electrical charge amplifier is especially qualified as interface for Dynapic and Dynasim.

The input leakage current of the micro processor must not be higher than I_I = 40nA for the pulse mode and not higher than I_{IL} = 0,1nA for the long-term mode.
The voltage supply (VSS = 0V, VDD = 2...5V) and the input voltage supply of the micro processor are virtually irrelevant, since mainly changes are recorded. The inputs must not show any Schmitt-Trigger characteristics and not be equipped with Pull Up resistors. The pulse duration should be adapted to the voltage threshold.

4.2 µP PIC16F84 as Interface for Dynasim

- The realization of an electrical charge amplifier with the aid of a micro processor can replace the interface ASIC DYSI-97S/ PS/ PSK, but only if the extremely high ohmic character of the circuit is taken into account.
- This circuit is especially qualified for applications where a certain amount of electrical charge has to be measured as signal threshold, that is especially for Dynasim.
- More detailed information in the datasheet *Dynapic and Dynasim Interface with Micro Processors*.