Dynapic and Dynasim Interface with Micro Processors

1 Introduction

The electrical charge amplifier is especially qualified as interface for Dynapic and Dynasim. Its realization with the aid of a micro processor and the method of the "oversampling" is specified hereafter.

2 Applications

The realization of an electrical charge amplifier with the aid of a micro processor can replace the interface ASIC DYSI-97PS /S, but only if it is considered to the extremely high ohmic characteristics of the circuit. This circuit is especially qualified for applications where a certain amount of electrical charge has to be measured as signal threshold, that is especially for Dynasim matrix. Half keys deliver half signals and several half keys have a large capacity. The resulting signal has a very low voltage.

3 Requirements

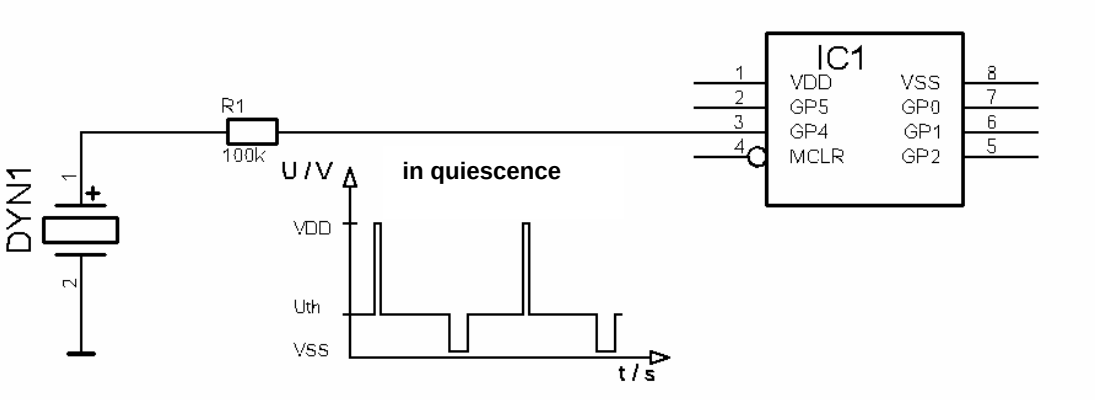
The input leakage current of the micro processor must not be higher than I_I = 40nA for the pulse mode and not higher than I_{IL} = 0,1nA for the long-term mode.
The voltage supply (VSS = 0V, VDD = 2...5V) and the input voltage supply of the micro processor are virtually irrelevant, since mainly changes are recorded. The inputs must not show any Schmitt-Trigger characteristics and not be equipped with Pull Up resistors. The pulse duration should be adapted to the voltage threshold.

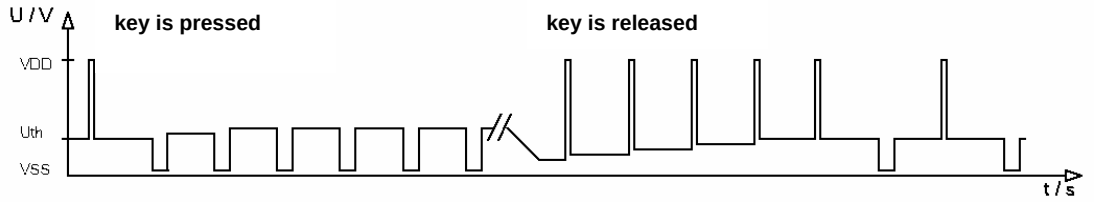
4 Description

A Dynapic or Dynasim signal is connected to the input/output of the micro processor with the aid of a serial resistor. This circuit combined with the adequate program has the same effect as an electrical charge amplifier. There are two different possibilities:

- When pressing the key the circuit gives out a pulse,
- The circuit should give out a signal as long as the key is pressed („long-time").

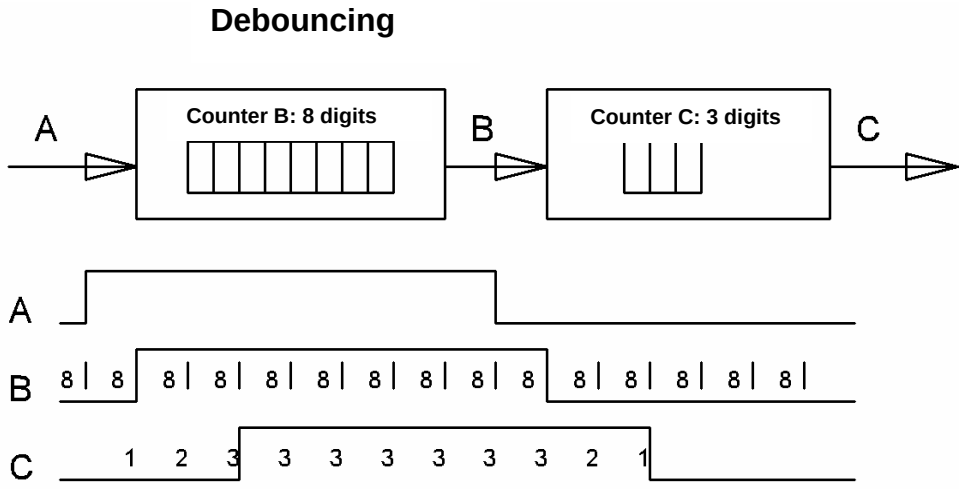
4.1 Pulse





The input signal is tested by the micro processor. If the input voltage signal is higher than the threshold U_{th}, the output is pulled to VSS = 0V for a short time. Combined with the serial resistor this corresponds to an extraction of the electrical charge out of the Dynapic or Dynasim element. If the input voltage signal is lower than the voltage threshold U_{th}, the output is pulled over the serial resistor to VDD = 5V for a short time. This corresponds to an infeed of electrical charge into the Dynapic or Dynasim element. Thus the voltage at this input and the attached Dynapic or Dynasim element should be controlled constantly to the voltage threshold U_{th} of the micro processor.

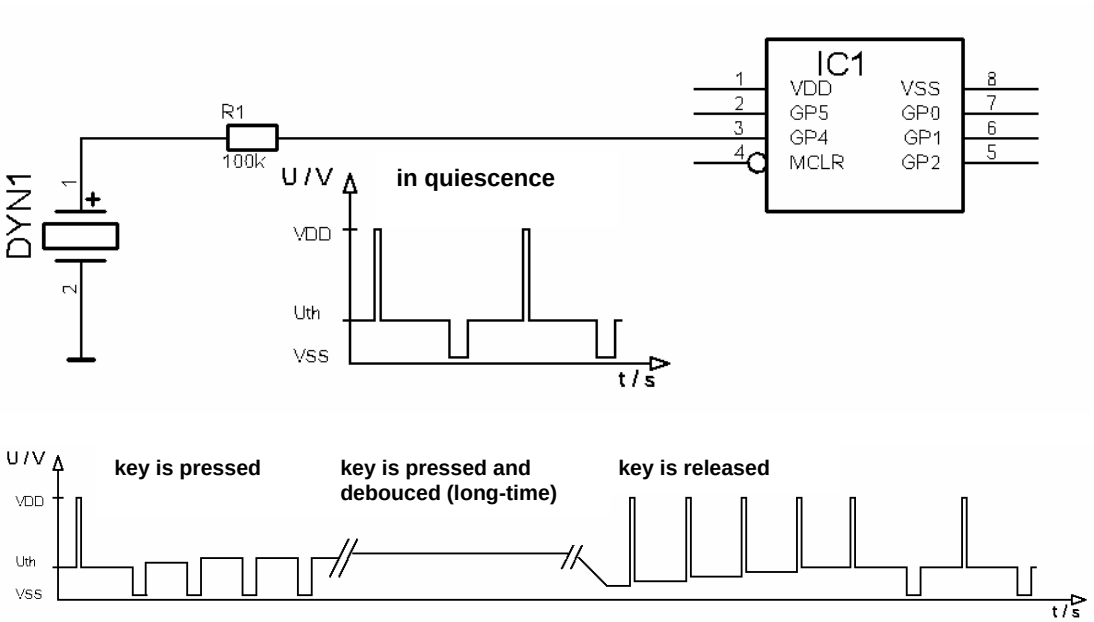
All inputs are scanned e.g. every 1,5ms and the number of the positive states are summed up. Every 8 scans the counter is compared, and if it holds 7 or 8, then a "1"-signal is passed on to the debouncing circuit. If the debouncing circuit gets the same signal at least three times in succession, the output changes respectively. If all 24 pulses are combined to a bloc the circuit becomes slower.



The debouncing filters out frequencies higher than approximately 30Hz. However, certain frequencies like f=667Hz (1:1,5ms) and multiples of this frequency may pose disorders due to the sampling technique used in this circuit. For this reason the scanning rate should be adjusted slightly in systems showing interferences due to such critical frequencies.

The threshold for the input signal is given by the amount of electrical charge that the input resistances dissipate in average during the time 8*3*1.5ms=36ms. This input charge threshold can be set through the duration of the pulse, during which the input/output is active. Since the threshold for TTL- compatible inputs for micro processors is approx. 1,2V, the extraction time for active "0" is set to the triple value of the infeed time for active "1". Thus the amount of electrical charge is about the same in both cases.

4.2 Long-Time



If the signal is identified to be active the inputs/outputs are only used as inputs until the input voltage falls under the voltage threshold U_{th} again or until the (programmable) time limit has expired. Setting the inputs/outputs to input has the effect that at the respective inputs no electrical charge is dissipated any more. Consequently a positive voltage can remain at the inputs as long as a key is pressed, which leads to a hold of the state switched on („long-time“).

5 Examples

Requirements:

1. On Port B there are n signals connected, EIN_DATA_B Bit n.
2. The debounced, valid signals are named with An.
3. Bn are the n pulse counters.
4. Z8 is a counter counting to 8.
5. Cn are the n debouncing counters.
6. ZEIT1 is the counter for the time-out with long-time.
7. 3 x 7 out of 3 x 8 pulses are needed for a valid signal.
8. The subroutine is called up every 1,5 ms, i.e. the minimal debouncing time is $3 \cdot 8 \cdot 1{,}5ms = 36ms$
9. Since the thresholds at the µP are approx. 1,2 V, the „1“-pulses are activated 1 µs and the „0“-pulses 3 µs.
10. With an input resistance of 100 kΩ the threshold is:

    Electrical charge for one pulse:
    $Q_{ein“0“}$ = 12µA * 3µs = 36pC
    $Q_{ein“1“}$ = 38µA * 1µs = 38pC

    Electrical charge for 3*8 = 24 pulses:
    $Q_{ein“0“}$ = 12µA * 3µs * 24 ≈ 0,9nC
    $Q_{ein“1“}$ = 38µA * 1µs * 24 ≈ 0,9nC

    In this case the threshold is set just under 1nC.

6 Structure charts

6.1 Structure chart for pulse

Procedure

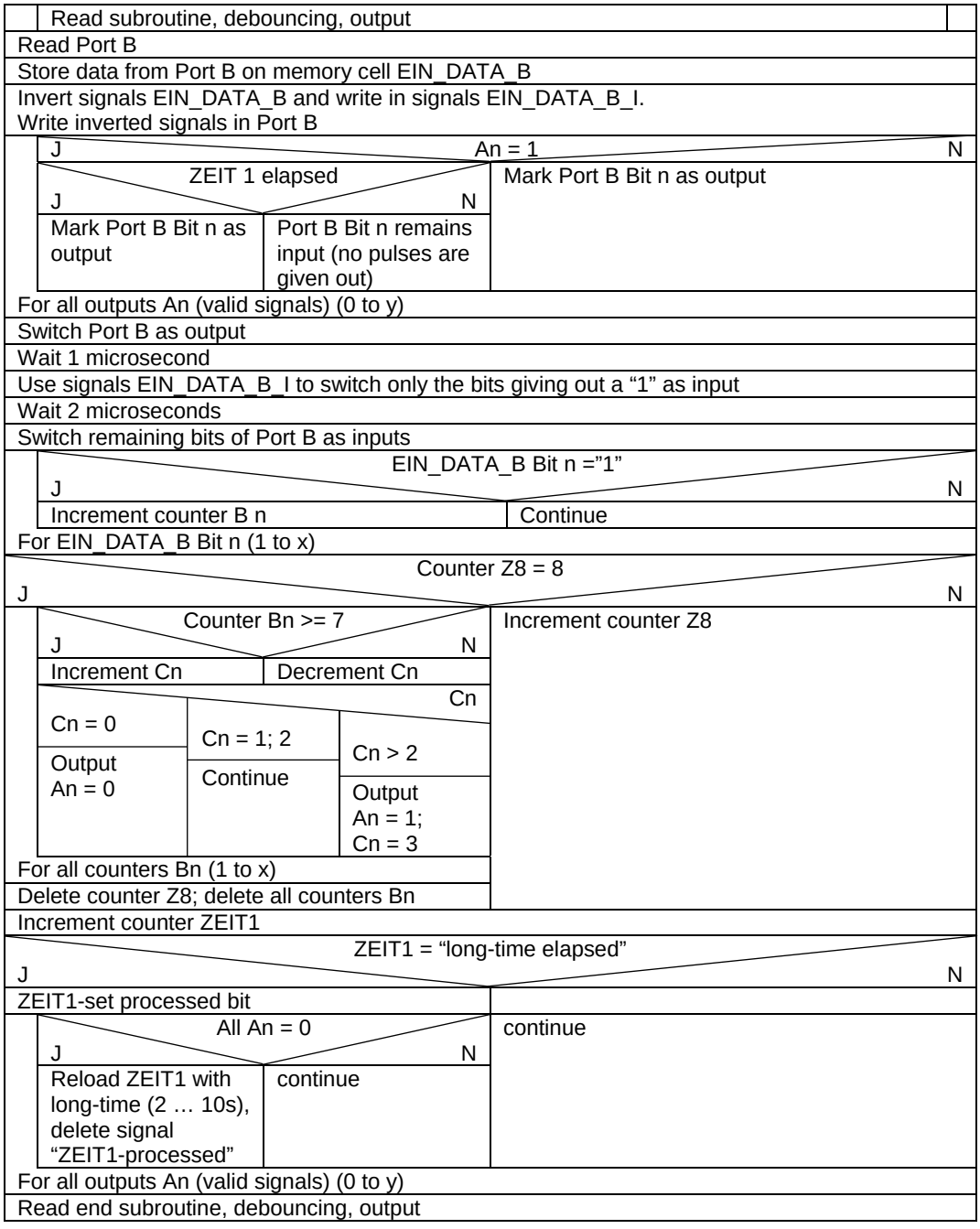
<table>
<tr><td colspan="3">Read subroutine, debouncing, output</td></tr>
<tr><td colspan="3">Read Port B</td></tr>
<tr><td colspan="3">Store data from Port B on memory cell EIN_DATA_B</td></tr>
<tr><td colspan="3">Invert signals EIN_DATA_B and write in signals EIN_DATA_B_I.
Write inverted signals in Port B</td></tr>
<tr><td colspan="3">Switch Port B as output</td></tr>
<tr><td colspan="3">Wait 1 microsecond</td></tr>
<tr><td colspan="3">Use signals EIN_DATA_B_I to switch the bits giving out a “1” as input</td></tr>
<tr><td colspan="3">Wait 2 microseconds</td></tr>
<tr><td colspan="3">Switch remaining bits of Port B as inputs</td></tr>
<tr><td colspan="3">EIN_DATA_B Bit n =”1”
J N</td></tr>
<tr><td colspan="2">Increment counter B n</td><td>Continue</td></tr>
<tr><td colspan="3">For EIN_DATA_B Bit n (1 to x)</td></tr>
<tr><td colspan="3">Counter Z8 = 8
J N</td></tr>
<tr><td colspan="2">Counter Bn >= 7
J N</td><td rowspan="5">Increment counter Z8</td></tr>
<tr><td>Increment Cn</td><td>Decrement Cn</td></tr>
<tr><td colspan="2">Cn</td></tr>
<tr><td>Cn = 0
Output
An = 0</td><td>Cn = 1; 2
Continue</td><td>Cn > 2
Output
An = 1;
Cn = 3</td></tr>
<tr><td colspan="2">For all counters Bn (1 to x)</td></tr>
<tr><td colspan="2">Delete counter Z8; delete all counters Bn</td><td></td></tr>
<tr><td colspan="3">Read end subroutine, debouncing, output</td></tr>
</table>

Legend:

EIN_DATA_B:	Input date, unprocessed
An:	Debounced, valid signals
Z8:	Counter counting to 8
Bn:	Pulse counters (one counter for each key)
Cn:	Debouncing counters (one counter for each key)

6.2 Structure chart for long-time

Procedure



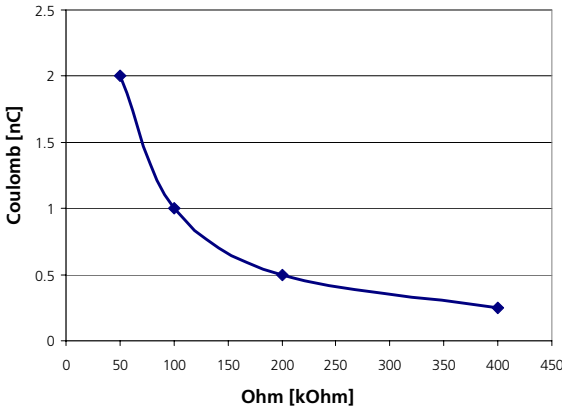
Legend:

EIN_DATA_B:	Input data, unprocessed
An:	Debounced, valid signals
ZEIT1:	Time-out for the long-time (2 ... 10 seconds)
Z8:	Counter counting to 8
Bn:	Pulse counter (one counter for each key)
Cn:	Debouncing counter (one counter for each key)

7 Adjustments

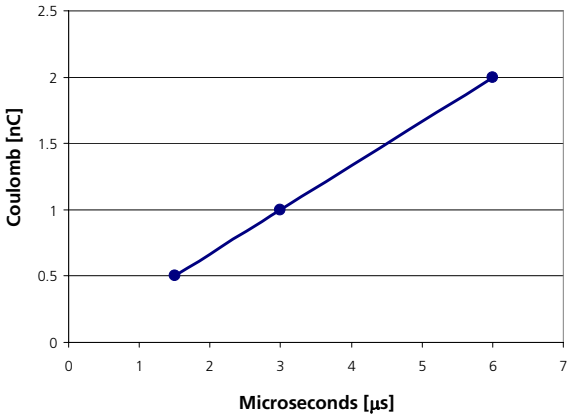
The threshold is set to approx. 1 nC.

Threshold in function of resistance



The threshold is inversely proportional to the value of the input resistance, in the example 100 kΩ. If the value of the resistance is e.g. doubled the average input current is halved. Consequently the value of the threshold is halved, that means the circuit becomes more sensitive.

Threshold in function of pulse time



The threshold is proportional to the value of the input resistance, in the example 3µs. If the time of the input pulse is e.g. doubled the average input current is doubled. Consequently the value of the threshold is doubled, that means the circuit becomes less sensitive.