Datasheet Dynapic and Dynasim Interface-Chip DYSI-97PS/PSK/S

1 Introduction

The Interface-ASIC DYSI-97PS /S /PSK is a complex interface chip in CMOS technology. It is especially designed to condition Dynapic and Dynasim signals. 1 up to 8 signals may be conditioned with one IC. Multiple circuits can be connected together to have more than 8 inputs. There are three different package options:

- the DYSI-97PS, supplied in SOIC28, MS-013-AE, has all options, particularly all 8 parallel outputs and one serial input and one serial output (in all applications with the DYSI-97PS the DYSI-97PSK can also be implemented),
- the DYSI-97PSK, supplied in QSOP/SSOP28, MO-137-AF, has all options, particularly all 8 parallel outputs and one serial input and one serial output,
- the DYSI-97S, supplied in SO16N, MS-012-AC, has only a serial output.

2 Applications

The Interface-ASIC DYSI-97PS/PSK/S is especially useful in applications that meet one or more of the following conditions:

- For Dynapic, if long-term mode is necessary.
- For Dynapic, in the case that a debouncing is necessary.
- For Dynapic, if there are different Dynapic elements, or if more than one Dynapic element per key is used.
- For Dynasim, because the Dynasim signals are in general much weaker than the Dynapic signals and for this reason it is difficult to process these signals without a special circuit.

3 Description

3.1 General description

- When the power is applied to the DYSI-97, the internal RESET is activated. All counters are set to 0 and all inputs are shorted to VSS for 55ms. Then the circuit begins to run under normal conditions.
- The 8 Dynapic and Dynasim inputs are internal switched with current source towards VDD and with current sinks toward VSS=0V. With the connected elements (Dynapic/Dynasim) the inputs will be regulated to the constant level of „V_{GUARD}“ = 0,6V. The inputs are scanned every 1.7ms and the number of positive states are summed up. Every 7 scans the counter is compared, and if it holds 6 or 7, then a “1“-signal is passed on to the debouncing circuit. The debouncing circuit output changes its state to a “1“ after 3 successive “1“ signals, or to a “0“ after 3 successive “0“ signals . Once an output is active, the related current source and the current sink are turned off, until the output switches back to the passive logical state or until the time limit of 24s has run out. The effect of the switching off of the current sources and the current sinks is that no charges are used on the related outputs any more. Consequently a positive voltage can remain on the outputs, which leads to the hold of the activated state („long-time“). This switching off of the current sources and the current sinks can be reduced to approximately 0.2s by activating the input “TLIM“. If after reactivating the current source/sinks the inputs are still on, these inputs will be shorted after 36s for 55ms to VSS, like the restart mode.
- The voltage threshold (0.6V) is generated inside the chip and fed out also as “GUARD“. This output, which is current limited to 4.5µA, is also an input, which can be connected with an external produced voltage, as a threshold voltage.
- The 8 output signals can be read out in parallel (active “0“), when the signal “ENABLE“ is active (“0“). Several DYSI-97PS can be connected in parallel, by connecting the related outputs together and activating the signals “ENABLE“ one by one.

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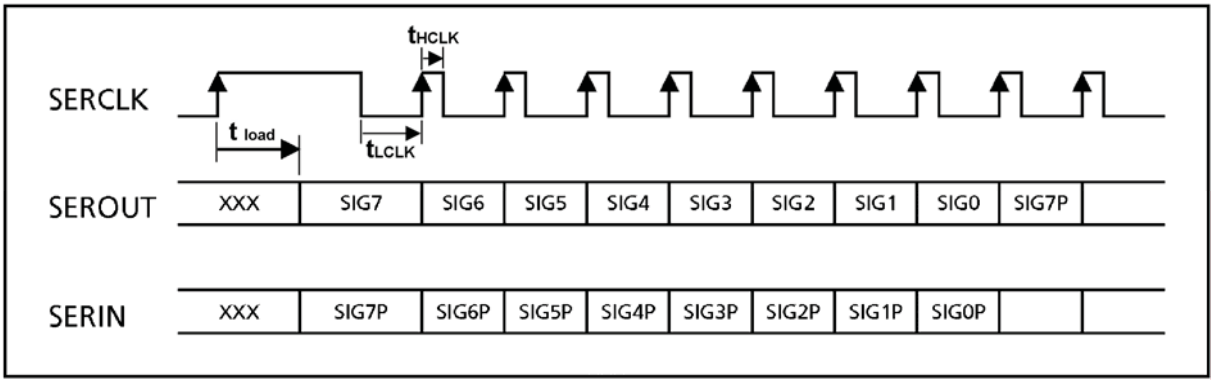
- The output signals can be read out also serially. The output shift register is loaded and clocked by activating „SERCLK“ and the data are shifted out to „SEROUT“. The output shift register is loaded by activating (set to “1“) “SERCLK“ for a minimum time t_{load}. After this time the first bit can be read on the output “SEROUT“, and then the other data are shifted out to “SEROUT“ on every positive edge of the “SERCLK“. Several DYSI-97PS can be connected in serial by connecting the “SEROUT“ of the previous DYSI-97PS to the “SERIN“ of the next one.



- The output signal “ACTIV“ is always active (“0“), if at least one key is active.
- The internal oscillator is run by connecting an external RC (R_{OSC} to VDD, C_{OSC} to VSS) on pin “OSC“, or an external clock frequency may be put in through a capacitor. The typical frequency should be 75kHz.
- A debouncing circuit filters out frequencies higher than approximately 30Hz. However, certain frequencies like f=586Hz (1:1.7ms) and multiples of this frequency may pose disorders due to the sampling technique used in this circuit. Therefore the oscillator frequency has to be shifted, if the system frequency is nearby the above mentioned frequencies.
- The threshold for the input signals is given by the amount of electrical charge that the current sinks dissipate in average during the time 7*3*1.7ms=36ms. This threshold can be set by connecting each of the inputs “DL“ and “DH“ either low ohmic (0Ohm ... 22kOhm) or high ohmic (330kOhm+/-30%) to either “1“ or “0“. This means there are 16 possible thresholds, and they form a geometric row with a factor of approximately 1,65 (Table 1).

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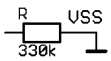
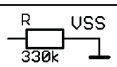
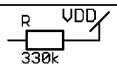
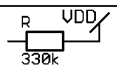
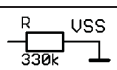
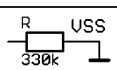
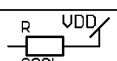
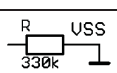
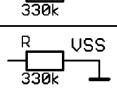
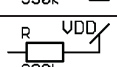
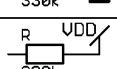
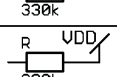
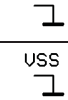
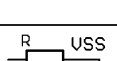
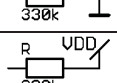
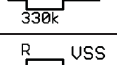
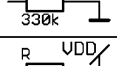
Table 1: Setting the threshold for a specific force

Range		Connect DL	Connect DH	Threshold	Current-Mean Value[1]	Force for Dynapic metallic	Force for Dynasim PC 0,5mm
0	A1			60pC	1,7nA		
1	A2			100pC	2,8nA		
2	A3			160pC	4,4nA		
3	A4			260pC	7,2nA		
4	B1			414pC	12nA		0.2 N
5	B2			700pC	19nA		0.35 N
6	B3			1,1nC	31nA		0.65 N
7	B4			1,8nC	50nA		0.9 N
8	C1			2,9nC	79nA	0.25 N	1.5 N
9	C2			4,9nC	135nA	0.4 N	2.5 N
A	C3			7,7nC	214nA	0.65 N	
B	C4			12,4nC	345nA	1.0 N	
C	D1			20nC	0,56µA	1.7 N	
D	D2			33nC	0,91µA	2.8 N	
E	D3			54nC	1,50µA	4.5 N	
F	D4			87nC	2,42µA	7.3 N	
All values are based on an oscillator frequency of 75kHz and a power supply of 5V.							

[1] The following current pulses are set by the sector:

- for sectors A & B I=70nA
- for sectors C & D I=3,4µA

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3.2 Description of the Pins

VDD	Positive supply voltage of the ASIC (typically VDD = 5V).
VSS	Negative supply voltage of the ASIC (typically ground = 0V).
INP0..INP7	Inputs to be connected to Dynapic and Dynasim switches. Unused inputs should be connected to VSS.
DH, DL	Input pins for charge threshold selection.
GUARD	Output and input with the threshold voltage, may serve as guard ring voltage. The threshold voltage may be altered by forcing this input to the desired voltage.
OSC	Oscillator input pin as node for the external RC (R_{OSC}=330kOhm connected to VDD, C_{OSC}=33pF connected to VSS), or for direct input of an external clock (only AC-coupled via a capacitor).
TLIM	Selection of the maximum time that the signal can be on when a switch is pressed. TLIM = "1" => t=24s. TLIM = "0" => t=0.2s.
SERIN	Serial input of the shift register. When multiple ASICs are connected together this input can be connected to the SEROUT of the previous ASIC. This allows to read all the switch states of all the ASICs as one stream. The input is active low with internal pull up resistor of 550kOhm.
SEROUT	Serial output of the shift register, active low. SEROUT = "0"=> the corresponding switches have been pressed.
SERCLK	Shift register clock. The shift register is first loaded and then the data are shifted on a positive edge of this input. There is a connection via a resistor of 300kOhm to the internal signal "ACTIV" (pull-up, if "ACTIV" is passive and pull-down if "ACTIV" is active).
ENOUT	Enable to activate the parallel outputs, active low with internal pull up resistor of 550kOhm.
OUT0...OUT7	Parallel output of the switch data, active low. OUTN="0" => the corresponding switches have been pressed.
ACTIV	Output to signalize that a key has been pressed, open drain, active low. ACTIV = "0" => a key has been pressed. The internal signal "ACTIV" is connected to SERCLK via a resistor of 300kOhm.

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4 Technical Data

4.1 Absolute Maximum Ratings

	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	-0.5	8	V	
Max. voltage on the general pins	V_i		VDD+0.5	V	
Max. voltage on the Dynapic signal pins	V_i		10	V	
DC input current (Dynapic signal pins)	I_i		+1 / -30	mA	
DC input current (general pins)	I_i		+/-30	mA	
Storage temperature range	T_{STOR}	-55	125	°C	
Lead temperature (soldering 10s)	T_L		260	°C	
Power dissipation	P_D		300	mW	

4.2 Operating Ratings

	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	2.7	5	6	V	
Quiescent device current	I_i		100	200	µA	V_{DD} = 5V
Operating temperature (only in "Pulse-Mode" => TLIM="0")	T_A	-40	25	+85	°C	
The input leakage currents rise with rising temperature, therefore the maximum signal duration of 24s is not guarantied at temperatures higher than 50°C.						

4.3 DC General Description

(All voltages referenced to VSS, VDD=5V)

Pin Name	Symbol	Characteristic	Min.	Typ.	Max.	Unit	Remarks
VDD	V	power supply		5		V	
SIG0...SIG7	V_i	threshold voltage		0.6		V	Set by V_{GUARD}
	V_{iclamp}	positive input clamp voltage	11	17		V	Independent of VDD
	I_{il}	input leakage current	-10	+/-1	+10	pA	Switch active, @ 25°C, not tested
	I_{in}	input current range (average)	1.67		2420	nA	Switch not active[2]
	I_{in_puls}	A & B range		+/-70		nA	
	I_{in_puls}	C & D range		+/-3.4		µA	
GUARD	I_{sink}			4.5		µA	
	V_{th_typ}			0.6		V	internal
	V_{th}		0.2		3.8	V	from external
digital inputs	V_{ith}	threshold voltage	1.5	2.5	3.5	V	
	I_{il}	input leakage current	-10		+10	nA	
	R_{pullup}	input pull up resistor		550		kΩ	SERIN & ENOUT
	R_{in}	input resistor		300		kΩ	SERCLK
outputs	V_{oh}	output high voltage	4.8			V	I_{out} =-1mA
	V_{ol}	output low voltage			0.2	V	I_{out} = 1mA
	I_{oh}	output high current	-6	-12		mA	V_{out} = 4V
	I_{ol}	output low current	6	12		mA	V_{out} = 1V
	V_{POR}	POR threshold	1.5		2.5	V	
	V_{ESD}	max. ESD voltage			2	kV	

[2] The input currents and therefore also the threshold vary proportionally with the power supply. That means that if the power supply is lowered, the input currents are reduced and therefore there is less charge needed to switch.

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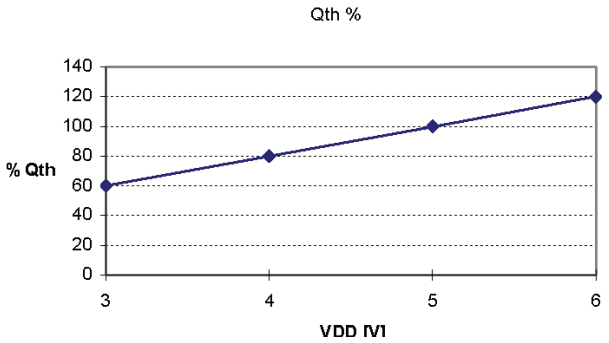
4.4 AC General Description

PIN Name	Symbol	Characteristic	Min.	Typ.	Max.	Unit	Remarks
OSC	f_{OSC}	clock frequency	20	75	300	kHz	

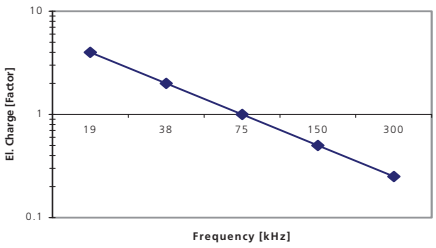
(All time values for a clock frequency of 75kHz)[3]

Pin Name	Symbol	Characteristic	Min.	Typ.	Max.	Unit	Remarks
SIG0...SIG7	f_{sample}	sample frequency		586		Hz	
	t_{delay}	turn on & turn off delay time	24		48	ms	
	$t_{debounce}$	debounce time			24	ms	Max. puls length, that is not detected.
	t_{lim1}	limit of the turn on time		24		s	TLIM="1"
	t_{lim0}	limit of the turn on time		0.15		s	TLIM="0"
	f_{max}	max. input signal frequency, that is not detected		30		Hz	at 50% duty cycle
	$f_{critical}$	lowest critical frequency	555	586	615	Hz	
	t_{reset}	reset time		55		ms	internal reset
SERCLK	t_{load}	time for shift register load	1.7			ms	
	t_{HCLK}	Clock pulse HIGH	0.5		500	µs	
	t_{LCLK}	Clock pulse LOW	0.5			µs	
	$t_{clk-out}$	time from clock to output	100	200	400	ns	
OUT0... OUT7	f_{clk}	shift register clock frequency		10	1000	kHz	
	t_{en}	output turn on time	10	35	100	ns	
	t_{hz}	output turn off time	10	20	100	ns	

Charge threshold as a function of power supply VDD



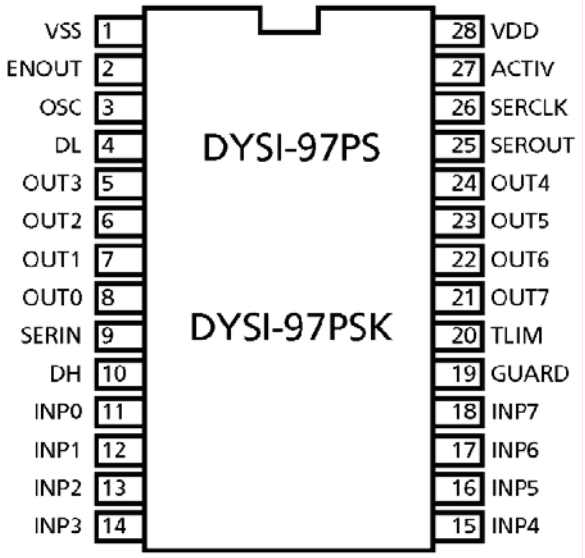
Charge threshold as a function of the oscillator frequency



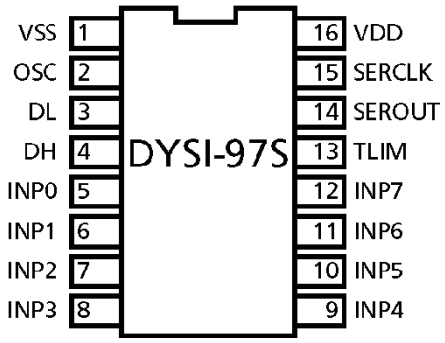
[3] All frequency and time values are related to a clock frequency of 75kHz. If the clock frequency is changed, the frequencies change proportionally and the times change in reverse proportion to the clock frequency.

4.5 PIN configuration (top view)

DYSI-97PS (SOIC28, MS-013-AE)
DYSI-97PSK (QSOP/SSOP28, MO-137-AF)



DYSI-97S (SO16N, MS-012-AC)



4.6 Mechanical outline

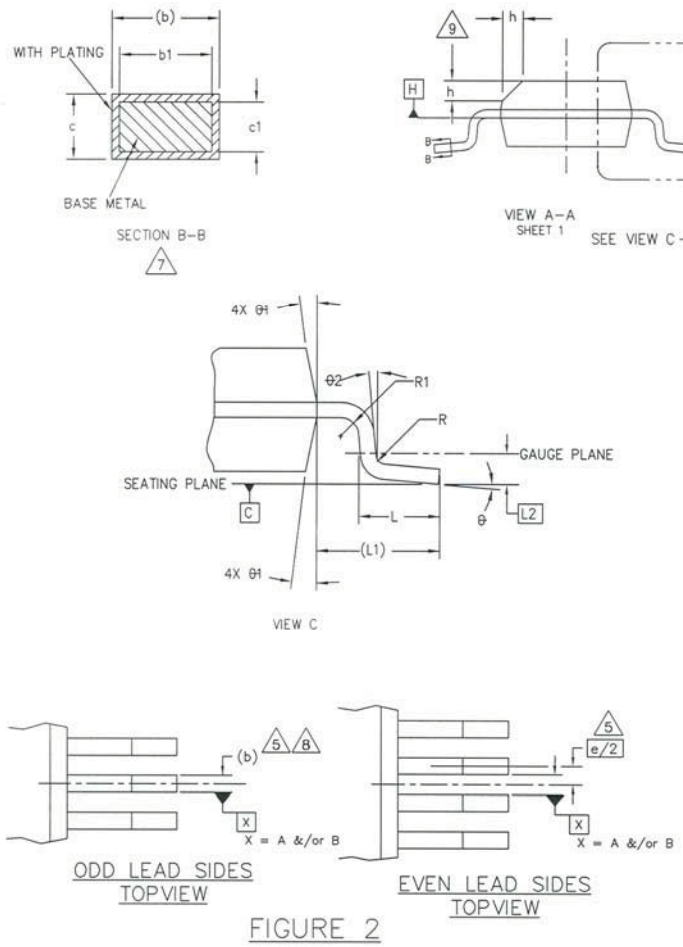
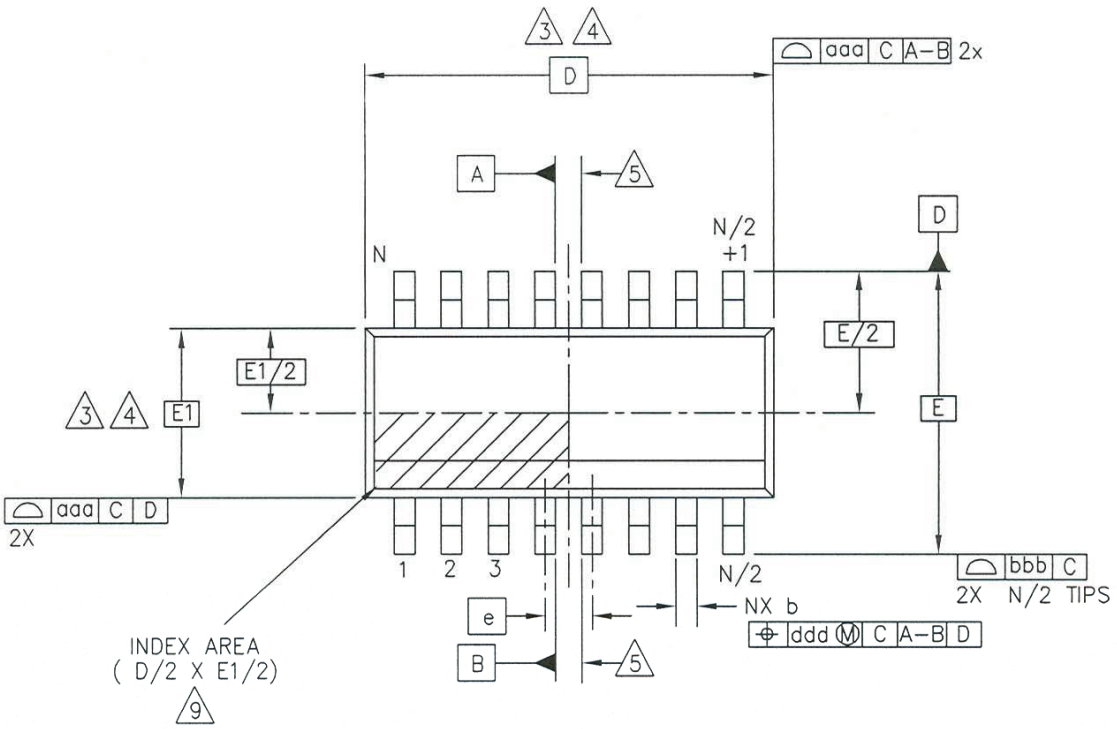
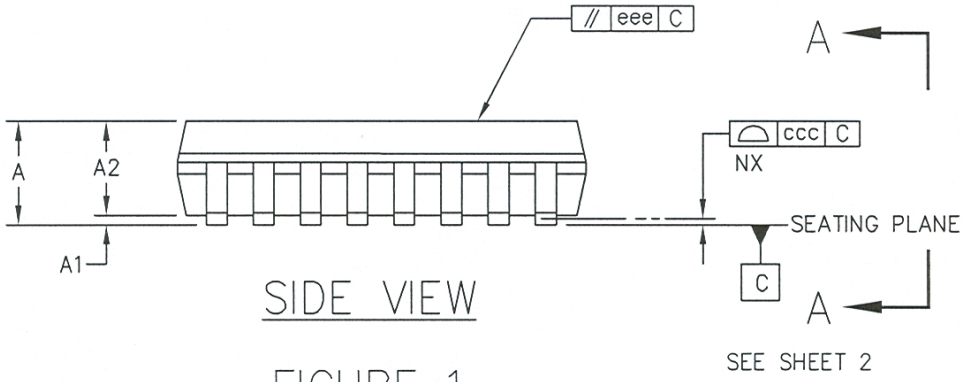


FIGURE 2



TOP VIEW



SIDE VIEW

FIGURE 1

SEE SHEET 2

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ALGRA

JEDEC MS-013-AE = SOIC28 = PS

SYMBOL	COMMON DIMENSIONS MIN	NOM	MAX	NOTE
A	2.35	–	2.65	
A1	0.10	–	0.30	
A2	2.05	–	2.55	
b	0.31	–	0.51	7,8
b1	0.27	–	0.48	7,8
c	0.20	–	0.33	7
c1	0.20	–	0.30	7
E	10.30 BSC			
E1	7.50 BSC			3,4
e	1.27 BSC			
L	0.40	–	1.27	
L1	1.40 REF			
L2	0.25 BSC			
R	0.07	–	–	
R1	0.07	–	–	
h	0.25	–	0.75	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11–614s			
ISSUE	D			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.10	
bbb	0.33	
ccc	0.10	
ddd	0.25	
eee	0.10	
fff	0.20	
NOTE	1,2	
REF	11–614s	
ISSUE	D	

VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	10.30 BSC	16	11.3–111	A
AB	11.55 BSC	18	11.3–111	A
AC	12.80 BSC	20	11.3–111	A
AD	15.40 BSC	24	11.3–111	A
AE	17.90 BSC	28	11.3–111	A
AF	9.00 BSC	14	11.4–225	B
NOTES	3,4	6		

JEDEC MO-137-AF = QSOP/SSOP28 = PSK

COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSIONS IN INCHES MIN	NOM	MAX	NOTE
A	0.053	–	0.069	
A1	0.004	–	0.010	
A2	0.049	–	0.065	
b	0.008	–	0.012	7,8
b1	0.008	0.010	0.011	7,8
c	0.006	–	0.010	7
c1	0.006	0.008	0.009	7
E	0.236 BSC			
E1	0.154 BSC			3,4
e	0.025 BSC			
L	0.016	–	0.050	
L1	0.041 REF			
L2	0.010 BSC			
R	0.003	–	–	
R1	0.003	–	–	
h	0.010	–	0.020	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11,11–627			
ISSUE	B			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.004	
bbb	0.008	
ccc	0.004	
ddd	0.007	
eee	0.004	
NOTE	1,2	
REF	11,11–627	
ISSUE	B	

VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	0.193 BSC	14	11,11–627	B
AB	0.193 BSC	16	11,11–627	B
AC	0.341 BSC	18	11,11–627	B
AD	0.341 BSC	20	11,11–627	B
AE	0.341 BSC	24	11,11–627	B
AF	0.390 BSC	28	11,11–627	B
NOTES	3,4	6		

JEDEC MS-012-AC = SOIC16N = S

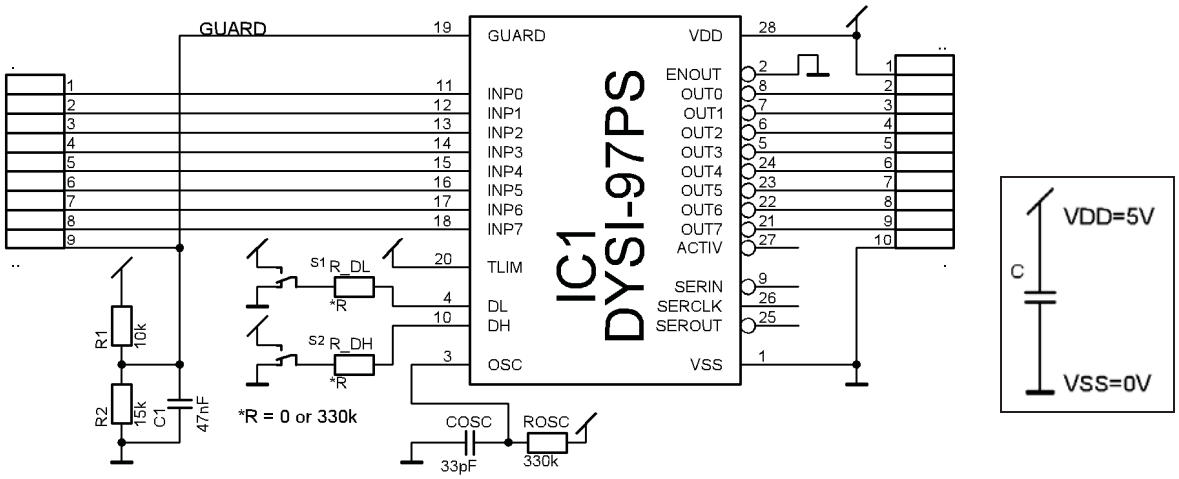
SYMBOL	COMMON DIMENSIONS MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
A2	1.25	–	1.65	
b	0.31	–	0.51	7,8
b1	0.28	–	0.48	7,8
c	0.17	–	0.25	7
c1	0.17	–	0.23	7
E	6.00 BSC			
E1	3.90 BSC			3,4
e	1.27 BSC			
L	0.40	–	1.27	
L1	1.04 REF			
L2	0.25 BSC			
R	0.07	–	–	
R1	0.07	–	–	
h	0.25	–	0.50	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11–613s			
ISSUE	D			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	
eee	0.10	
NOTE	1,2	
REF	11–613s	
ISSUE	D	

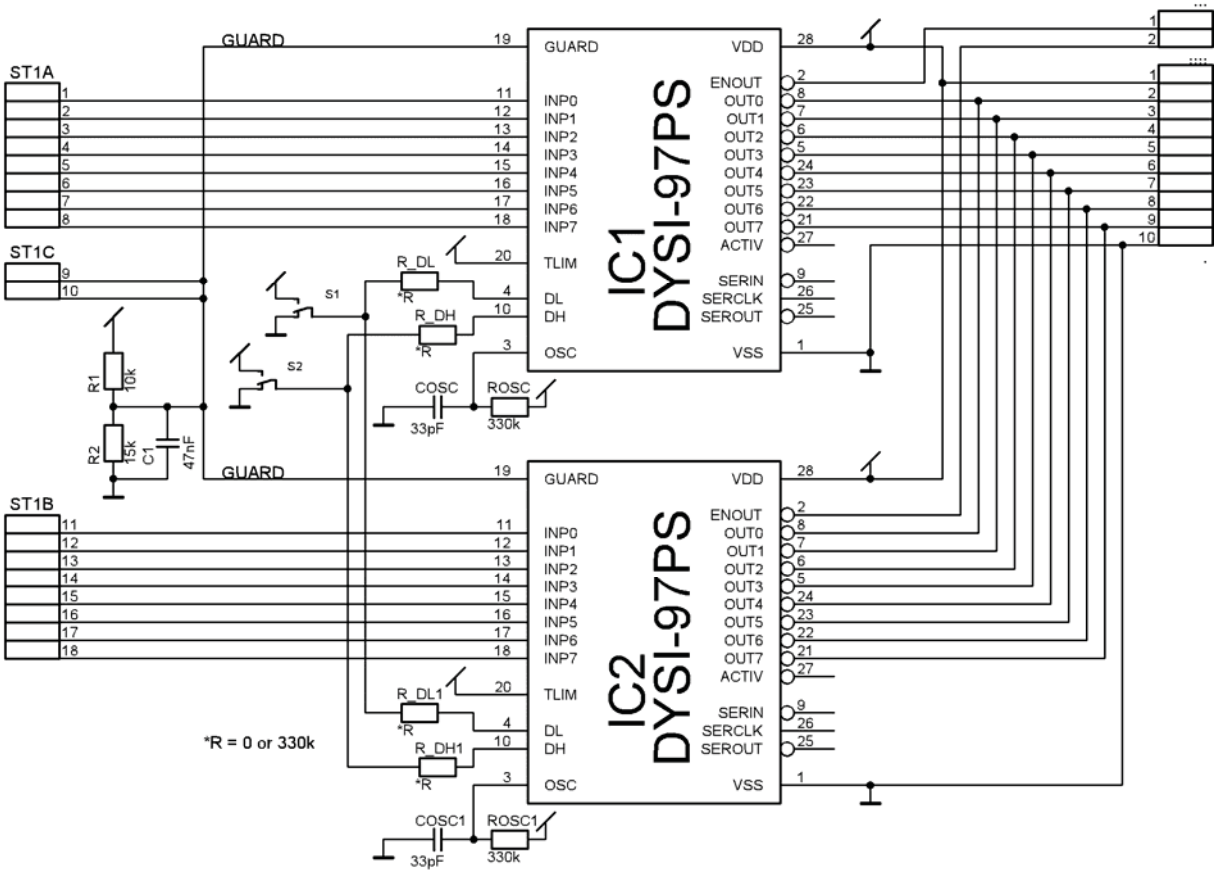
VARIATION	SYMBOL D	N	REFERENCE	ISSUE
AA	4.90 BSC	8	11.3–103	A
AB	8.65 BSC	14	11.3–103	A
AC	9.90 BSC	16	11.3–103	A
NOTES	3,4	6		

5 Examples

5.1 Example for 8 signals with a parallel output Dynapic



5.2 Example for more than 8 signals with a parallel output Dynapic



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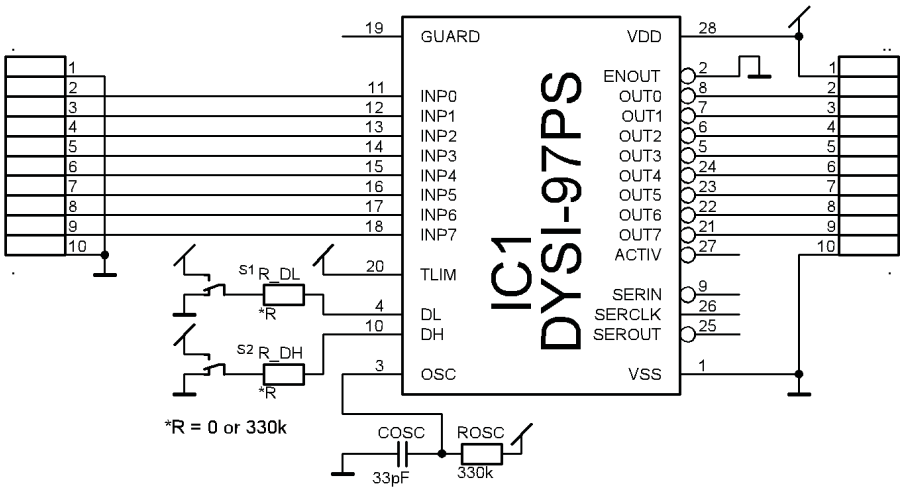
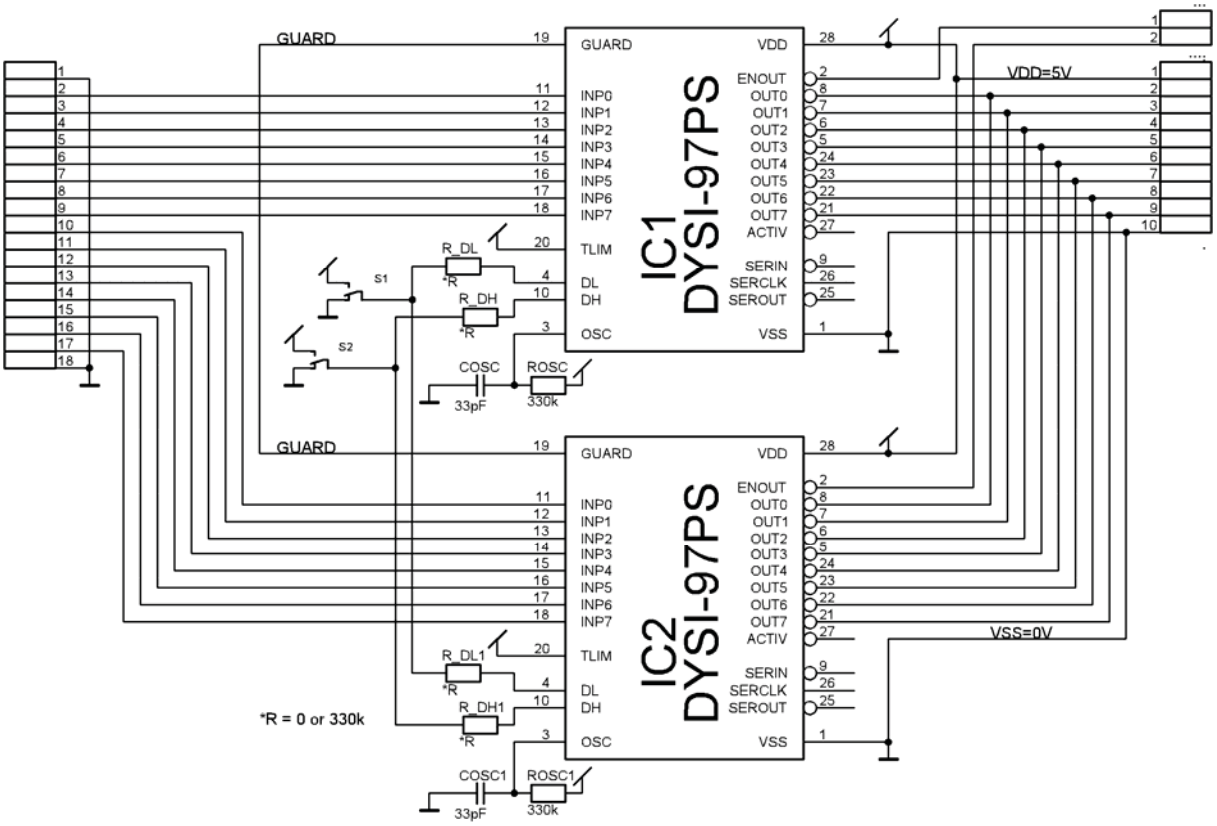
5.3 Example for 8 signals with a parallel output Dynasim



5.4 Example for more than 8 signals with a parallel output Dynasim



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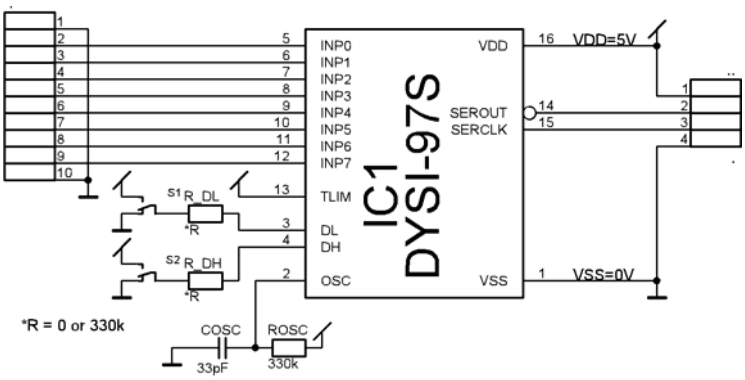
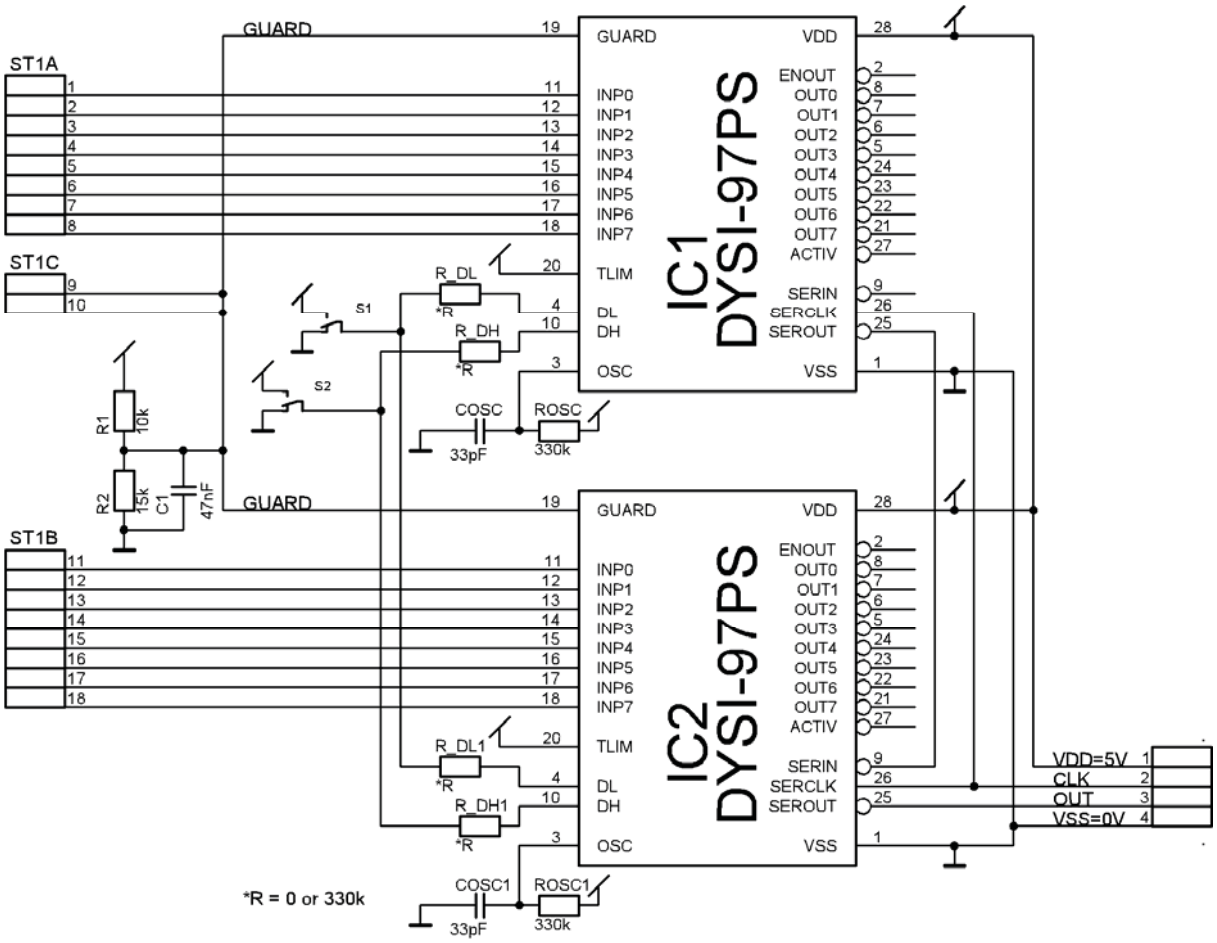
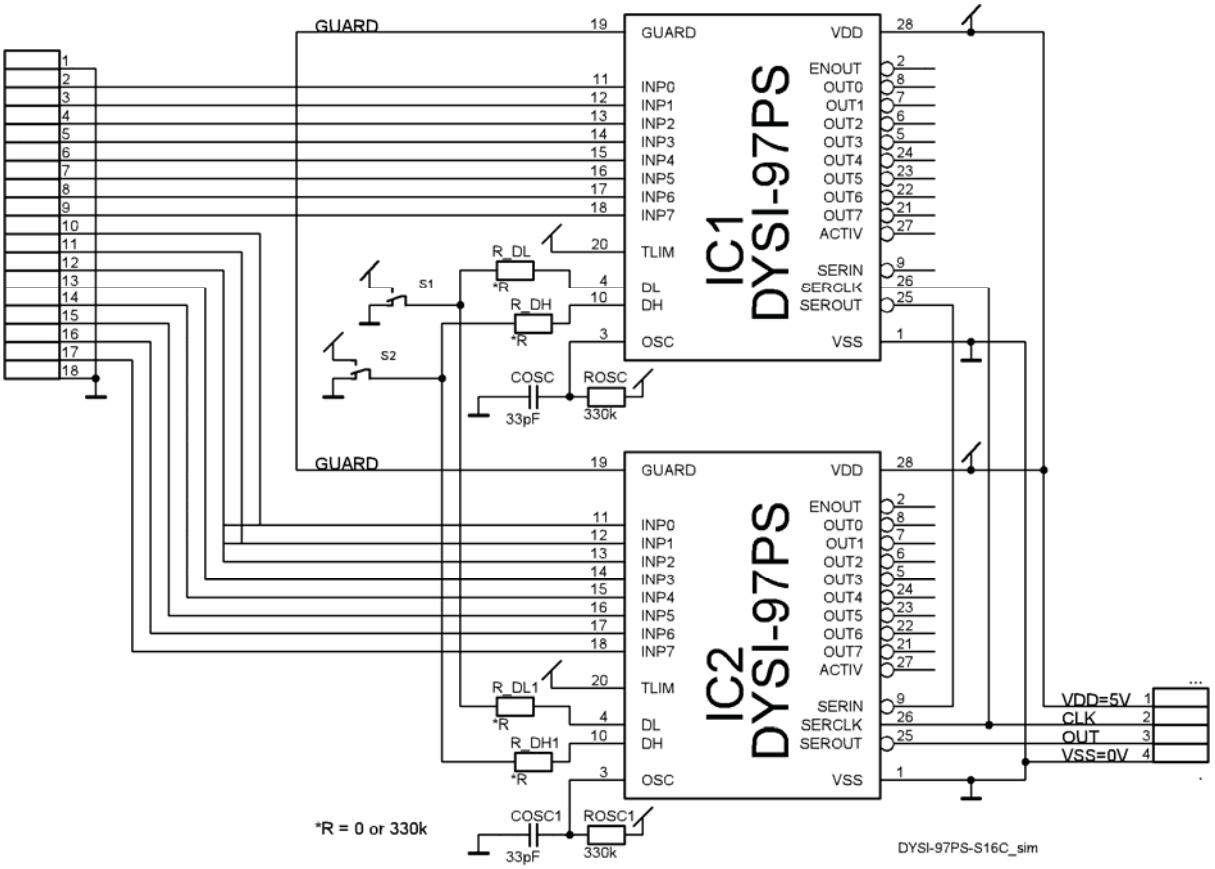
5.5 Example for 8 signals with a serial output Dynapic and Dynasim



5.6 Example for more than 8 signals with a serial output Dynapic



5.7 Example for more than 8 signals with a serial output Dynasim



6 Optional circuits

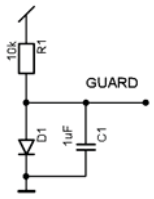
6.1 Optimization of the EMC behavior

6.1.1 Changing of the oscillator frequency

If the standard circuit of the DYSI-97 is not EMC-stable enough, the oscillator frequency can be reduced. For this purpose the oscillator R_{OSC} is increased from 330kΩ to 470kΩ, so the frequency is reduced from 75 kHz to approx. 52 kHz. This causes a rise of the thresholds and debouncing time of approx. 40%. The advantage of this circuit is that it becomes electrically more robust, without influencing the hardness of the keys tangibly. But the keys can not be activated by a short knock/pressing any more.

6.1.2 Changing of the guard circuit

In certain applications the circuit of the guard line, which is lead to the keyboard, proves to be not EMC-stable enough. In these cases the following circuit can be an improvement.

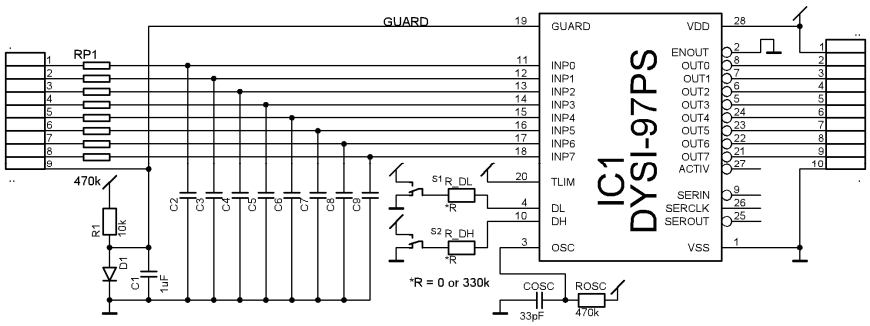


The diode D1 can be a single signal diode, several signal diodes or a Z-Diode. The voltage GUARD should be between 0.7 V and 3 V.

6.1.3 Adding of capacitors

In certain applications the circuit of the signal inputs with capacitors and/or resistances can be necessary.

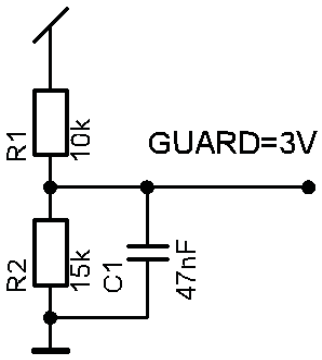
The following scheme shows a circuit with all the above mentioned optional EMC improvements.



6.2 Optional circuit only for Dynapic

If a Dynapic key is pressed very hardly, on certain conditions (high voltage signal) the circuit DYSI-97 can produce long-time signals. This effect is caused by the fact that the diode protecting the input discharges electricity towards 0V, if the input voltage becomes approx. 0,4V more negative than VSS=0V. Thereby the piezo element is charged positively and this charging can be valued as a signal. This effect can be avoided extensively by one of the following two measures.

1. The guard voltage is increased, e.g. to 3V. Consequently the quiescent voltage on the inputs is also increased from 0,6V to 3V and an input diode is only conductive when the signal voltage is more negative than approx. 3,4V, related to the guard voltage. At the same time the guard voltage is used as a common conductor for the keyboard, so that in quiescence no voltage lies against the piezo elements.



2. Since with the DYSI-97S the guard voltage is not available, a possible issue must be solved with the circuit of the signal inputs. Therefore a resistance of 470kΩ per input can be connected together in serial and a capacitor of 4,7nF towards VSS can be connected in parallel. On the one hand the current is limited by the input diode and on the other hand the impulse-shaped currents of the input circuits are smoothed.